

### REMARKS

Claims 1 through 20 remain pending in the present case.

### DRAWINGS

Applicant is submitting separate drawing amendments concurrently with the present response.

Applicant has amended Figure 1 to include a legend designating the figure as related art.

Applicant has added Figure 7 to show an information configuration core including a transmit channel comprising a phase aligner, encoder, and serializer. Figure 7 also shows the information configuration core includes a receive channel comprising a deserializer, framer, decoder, and elasticity buffer.

Applicant has added Figure 6A and 6B to show the limitations of Claim 20.

### SPECIFICATION

Applicant has amended the specification to refer to the patent number 6,594,325.

Applicant has amended the specification to include a description of added Figures 6A, 6B (the first paragraph on page 16) and Figure 7 (the second paragraph on page 11). The description amendments corresponding to figures 6A and 6B are supported by originally filed claim 20 and the description amendments corresponding to figure 7 are supported by originally filed Claims 4 and 5. Applicant respectfully asserts no new subject matter has been added.

### 112 REJECTIONS

The present Office Action rejects claims 4, 5, 20, 12, and 20 for failing to particularly point out and distinctly claim the subject matter applicant regards as the invention.

Applicant has amended Claims 4 and 5 to include structural connections.

Applicant has amended Claim 10 to remove the reference to DC.

Applicant has amended Claim 12 to read "a single substrate" instead of "said single substrate".

Applicant respectfully submits the reference in Claim 20 to "a transmit channel" and "a receive channel" does not have an antecedent conflict with Claim 17.

### 102 REJECTIONS

In the above referenced Office Action, Claims 1-7, 9, and 11-20 are rejected under 35 USC 102(e) as being anticipated by Dodd et al. (U.S. Patent 6,530,006). Applicant has reviewed the Dodd et al. reference and, for the following rationale, Applicant respectfully asserts that the present invention is not anticipated nor rendered obvious by the Dodd et al. reference.

In regards to Claims 1, 11 and 17, Applicant respectfully contends that the Dodd et al. reference fails to teach an interface and memory array on a single substrate with interfaces operating at different rates. For example, amended Claim 1 recites in part (emphasis added):

...a system interface for communicating with a system controller at a first communication rate, ... and

a memory array interface for communicating with a memory array at a second communication rate, ... wherein said memory array is included on a same substrate as said high speed serial memory interface system.

Applicant respectfully asserts that the Dodd et al. reference does not teach or suggest memory array and high speed serial memory interface included on the same substrate with a system interface for communicating at one rate and a memory array interface for communicating at another rate.

Applicant respectfully asserts that to the extent the Dodd et al. reference may mention an input clock is driven from the memory controller 110 or an external source [Col. 4, line 67 – Col. 4 line 5], the Dodd et al. reference does not teach a system interface for communicating with a system controller at a first communication rate, and a

memory array interface for communicating with a memory array at a second communication rate. Furthermore, to the extent the Dodd et al. reference may mention the clock 300 controls the output clock 20 to have the same phase as the input clock 10 [Col. 4, lines 10 –12 and Col. 5, lines 25 – 30], Applicant respectfully asserts that the Dodd et al. reference teaches away from the present invention by indicating Dodd et al. is adjusting a phase delay in a single clock signal [Col. 4, lines 57 – 58] and not two different clock rates.

To the extent the Dodd et al. reference may mention external (discrete) buffers are utilized to allow different voltages and frequencies to be used for the memory controller 110 and memory devices 130 – 145 and 170 – 185 [Col. 3 lines 43 – 45], Applicant respectfully asserts the Dodd et al. reference does not teach a system interface for communicating with a system controller at a first communication rate, and a memory array interface for communicating with a memory array at a second communication rate, wherein the memory array is included on the same substrate as said high speed serial memory interface system.

Applicant respectfully asserts Claims 2 – 10, 12 – 16 and 18 - 20 are allowable as depending from an allowable independent Claims 1, 11 and 17 respectively.

With regard to Claim 2, the present Office Action alleges it is clear the system interface of the Dodd et al. reference comprises a serial read data port, serial write data port and serial address data port that communicate serial read, serial write and serial address information in accordance with a first synchronized clock signal. To the extent the Dodd et al. reference may mention that the connection lines are represented as a

single line to the buffer 120, and to the memory device 130 – 145, and each represented line may in fact be a plurality of lines [Col. 2 lines 54 –57], Applicant respectfully asserts that Dodd et al. does not teach a system interface for communicating with a system controller at a first communication rate and a memory array interface for communicating with a memory array at a second communication rate, where said system interface comprises a serial read data port, a serial write data port and a serial address data port. Applicant also respectfully asserts the Dodd et al. reference does not mention serial information and/or a serial port.

With regard to Claim 3, the present Office Action alleges it is clear the memory interface of the Dodd et al. reference comprises a parallel transmit port, parallel receive port, a parallel address port and a control port that communicate information in accordance with a second synchronized clock signal. To the extent the Dodd et al. reference may mention that the connection lines are represented as a single line to the buffer 120, and to the memory device 130 –145, and each represented line may in fact be a plurality of lines [Col. 2 lines 54 –57], Applicant respectfully asserts that Dodd et al. does not teach a system array interface for communicating with a system controller at a first communication rate and a memory array interface for communicating with a memory array at a second communication rate, where said memory array interface comprises a parallel transmit port, parallel receive port, a parallel address port and a control port. Applicant also respectfully asserts the Dodd et al. reference does not mention parallel information and/or a parallel port.

With regard to Claim 4, the present Office Action alleges it is clear the interface system of Dodd comprises a phase aligner 300. To the extent the Dodd et al. reference

may mention clock circuit 300 controls the output clock 20 to have the same phase as the input clock 10 [Col. 4, lines 11 – 12], Applicant respectfully asserts the Dodd et al. reference does not teach a phase aligner for aligning signals forwarded from a memory array interface as claimed in the present application. The present Office Action also alleges it is clear the Dodd et al. reference system interface must include an encoder. Applicant respectfully asserts that Dodd et al. does not teach an encoder for encoding signals forwarded from a memory array interface as claimed in the present application. The present Office Action alleges it is clear that signals received from memory devices 130/13 or 1-8 of the Dodd et al. reference must be serialized. Applicant respectfully asserts the Dodd et al. reference does not teach a serializer for serializing signals received from the memory array interface as claimed in the present application.

With regard to Claim 5, the present Office Action alleges the Dodd et al. reference teaches serial data is converted to parallel data based upon the Office Action discussion of claims 2 and 3, and it is clear the serial data must be deserialized. In accordance with the rationale presented above, Applicant respectfully asserts the Dodd et al. reference does not teach serial data is converted to parallel data. Applicant respectfully reiterates the Dodd et al. reference does not mention the words “serial” and/or “parallel”. In addition, to the extent the Dodd et al. reference may mention clock circuit 300 controls the output clock 20 to have the same phase as the input clock 10 [Col. 4, lines 11 – 12], Applicant respectfully asserts the Dodd et al. reference does not teach a phase aligner for aligning signals forwarded from a memory array interface as claimed in the present application. The present Office Action alleges it is clear the Dodd et al. reference teaches a framer. Applicant respectfully asserts the Dodd et al. reference does not teach a framer for framing information received from the system

interface to its byte boundary as claimed in the present application. The present Office Action alleges it is clear the Dodd et al. reference teaches a decoder. Applicant respectfully asserts the Dodd et al. reference does not teach a decoder for decoding information received from the system interface as claimed in the present application. The present Office Action alleges it is clear the Dodd et al. reference teaches an elasticity buffer. Applicant respectfully asserts the Dodd et al. reference does not teach an elasticity buffer for buffering information received from the system interface as claimed in the present application.

With respect to Claim 6, the present Office Action alleges the memory clock of the Dodd et al. reference is slower than the controller clock. To the extent the Dodd et al. reference may mention the input clock 10 is either driven from the memory controller 110 or from an external source [Col. 3 lines 67 – Col. 4 line 5], Applicant respectfully asserts the Dodd et al. reference does not teach the memory array interface operates at a second clock speed that is slower than a first clock speed of operations at the system interface. In addition, Applicant respectfully asserts the Dodd et al. reference emphasis teaches away from the present invention by indicating the input clock to the memory array is the same as the controller clock [Col. 3 lines 67 – Col. 4 line 5] and when the PLL is locked the frequency and phase of the output signal are the same as those of the input signal [Col. 5, lines 28 – 30].

With respect to Claim 7, the present Office Action makes a reference to “note” the address and control/command buses and data buses to and from memory devices (130/135 or 1-80). To the extent the Dodd et al. reference may show address and control/command buses and data buses to and from memory devices, Applicant

respectfully asserts the Dodd et al. reference does not teach a memory array interface deals with the reading and writing of data to and from a memory array with address and control buses as claimed in the present application.

With respect to Claims 13 and 14, the present Office Action alleges the advantages are irrelevant and do not define any step/structure that differs from the Dodd et al. reference. Applicant respectfully asserts Claim 13 includes defined limitations including the single substrate is a well controlled environment and capacitive flux in the point to point connections is manageable. Applicant respectfully asserts Claim 13 includes defined limitations including signals with low voltage swings that produce very low noise potential on each line.

With respect to Claims 11, 12, and 16 the present Office Action refers to the allegations discussed above. Applicant respectfully reasserts the Dodd et al. reference does not teach the present claimed invention as discussed above. The present Office Action also notes the Dodd et al. reference allegedly discloses a single chip memory module integrated high speed interface system. To the extent the Dodd reference may mention a buffer structure and memory devices are housed within a memory module 150 [Fig. 5 and Col. 5, lines 60 – 65], Applicant respectfully asserts the Dodd et al. reference does not teach a single chip memory module integrated high speed serial interface system comprising a memory module array and a high speed serial memory interface system as claimed in the present application. In addition, Applicant respectfully asserts that the Dodd et al. reference teaches away from a single chip memory module by indicating the memory module 150 of the Dodd et al. reference is a

board with separate memory devices 130 – 135 and separate buffer 120 [Fig. 2 and Col. 3, lines 20 – 45].

With regard to Claim 15 the present Office Action alleges the Dodd et al. reference teaches the data and address bits are provided synchronously upon a clock signal edge. Applicant respectfully asserts the Dodd et al. reference does not teach data and address bits are provided synchronously upon a clock signal edge as claimed in the present application.

With regard to Claims 17 – 20, the present Office Action alleges it is clear that one using the system of the Dodd et al. reference would have performed the same steps set forth in claims 17 – 19. Applicant respectfully asserts the Dodd et al. reference does not teach a high speed serial memory interface method as claimed in the present application.

### 103 Rejections

The present Office Action indicates Claims 8 and 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over the Dodd et al. reference. Applicant respectfully asserts that the present invention is neither shown nor suggested by the Dodd et al. reference.

Regarding Claim 8, the present Office Action acknowledges that the Dodd et al. reference fails to teach double data rate (DDR). The present Office Action alleges that DDR clock is well known and it would have been obvious to one of ordinary skill in the

art to use DDR. Even if the present Office Action allegation that DDR is well known is correct, Applicant respectfully asserts a high speed serial memory interface system wherein communications are synchronous to a system clock at double rate clocking as claimed in the present application is not taught by the Dodd et al. reference nor obvious.

Regarding Claim 10, the present Office Action acknowledges that the Dodd et al. reference fails to teach an 8B/10B encoder. The present Office Action alleges that an 8B/10B encoder is well known and it would have been obvious to one of ordinary skill in the art to use an 8B/10B encoder. Even if the present Office Action allegation that an 8B/10B encoder is well known is correct, Applicant respectfully asserts a high speed serial memory interface system including 8B/10B encoding as claimed in the present application is not taught by the Dodd et al. reference nor obvious.

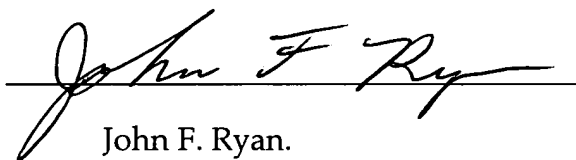
## CONCLUSION

In light of the above remarks, Applicant respectfully requests allowance of the remaining Claims. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO

Date: 8/18 2004

A handwritten signature in black ink, reading "John F. Ryan", is written over a horizontal line.

John F. Ryan.

Reg. No. 47,050